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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10081109	02/25/2002	257	776	2815	Eugene Lee

**APPLICANTS: Sakamoto Shinsuke; Inbe Yasuo; Yaginuma Masakazu; Horikawa Kazunari; Sei Toshikazu;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A CON OF 09/527,563 03/16/2000

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 11-069907 03/16/1999

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☒ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☒ yes ☐ no	4329.2270-01
Verified and Acknowledged Examiners's intials		

TITLE : Semiconductor integrated circuit device and wiring arranging method thereof

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Eugene Lee **Assistant Examiner**	**CLAIMS ALLOWED** Total Claims: 11 — Print Claim for O.G: 1
ISSUE FEE Amount Due / Date Paid		**DRAWING** Sheets Drwg.: 2 — Figs.Drwg.: 4 — Print Fig.: 1, 2
☐ **TERMINAL DISCLAIMER**	**Primary Examiner** **PREPARED FOR ISSUE**	**Applicati n Examiner**

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